MATH COPROCESSOR

ABSTRACT OF THE DISCLOSURE

A math coprocessor 1300 includes a multiply-accumulate unit 1600. Multiplier-accumulate unit 1600 includes a multiplier array 1603 for selectively multiplying first and second operands, the first and second operands having a data type selected from the group including floating point and integer data types. An adder 1604 selectively performs addition and subtraction operations on third and fourth operands, the third and fourth operands selected by multiplexer circuitry from the contents of a set of associated source registers, data output from multiplier array 1603 and data output from adder 1604.

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